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UTILITY PATENT APPLICATION TRANSMITTAL

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Attorney Docket No.	4161US (98-1265)
First Inventor or Application Identifier	Warren M. Farnworth
Title	METHOD AND APPARATUS OF INTERPOSING VOLTAGE REFERENCE TRACES BETWEEN SIGNAL TRACES IN SEMICONDUCTOR DEVICES
Express Mail Label No.	EL500249732US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

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2. [X] Specification [Total Pages 16] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 5]
4. Oath or Declaration [Total Pages 1]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***
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ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [X] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
12. [ ] Preliminary Amendment
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APPLICATION FOR LETTERS PATENT

for

METHOD AND APPARATUS OF INTERPOSING VOLTAGE REFERENCE TRACES BETWEEN SIGNAL TRACES IN SEMICONDUCTOR DEVICES

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METHOD AND APPARATUS OF INTERPOSING VOLTAGE REFERENCE TRACES BETWEEN SIGNAL TRACES IN SEMICONDUCTOR DEVICES

BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates generally to the reduction or elimination of "cross-talk" between semiconductor device signal traces by interposing a grounding element between the signal traces. More particularly, the present invention relates to interposing a grounding element between printed circuit board traces and vias to minimize or eliminate mutual coupling between signal conductors.

State of the Art: Cross-talk between two adjacent conductive signal traces is a result of electrostatic and electromagnetic coupling between the conductive traces. Electrostatic and electromagnetic coupling is related to the impedance of a signal trace such that as mutual coupling increases, impedance increases. Cross-talk between signal traces is undesirable because it may cause signal delays and interference with signals transmitted through the signal traces. The primary factors affecting cross-talk include the surface area of the signal trace directed to an adjacent signal trace, the distance between the signal traces and the dielectric constant (ϵ_r) of the material between the signal traces. Air has a dielectric constant of 1, while printed circuit board resin conventionally has a dielectric constant of between 3 and 4. In general, coupling and cross-talk between two adjacent conductive signal traces increases as the facing surface areas of the traces increases, as the dielectric constant of the material between the signal traces increases, and as the distance between the signal traces decreases.

With the continuous desire of manufacturing smaller semiconductor devices, the distances between signal traces have necessarily been reduced, and multiple-layer and specially fabricated semiconductor and printed circuit board materials have been used to compensate for the electromagnetic coupling caused by closer conductors. One approach to canceling the electromagnetic coupling of a bias source in an electronic device is disclosed in U.S. Patent 4,349,848 to Ishii et al. (Sep. 14, 1982). Ishii et al. uses impedance cancellation methods to cancel mutual coupling between signal traces by placing bias currents having opposite phases in two separate signal traces running parallel

to each other. In this way, the electromagnetic fields from the two signal traces cancel each other out. This approach, however, is not conducive to all signal traces, and is particularly not conducive to signal traces which do not run in parallel or do not carry complementary signals.

Another approach known in the art for reducing electromagnetic coupling between signal traces is to alternatively design printed circuit board or semiconductor materials which inherently reduce coupling. U.S. Patent 5,785,789 to Gagnon et al. (Jul. 28, 1998) discloses multilayer circuit board structures comprising discrete, partially-cured, microsphere-filled resin layers. By specially fabricating circuit board layers, the dielectric constant of the printed circuit board is lowered, resulting in lower conductivity and coupling through the circuit board material. U.S. Patent 3,990,102 to Okuhara et al. discloses a semiconductor integrated circuit comprising a dielectric isolation region and both a high resistivity layer and a low resistivity layer adjacent to monocrystalline regions to shield electrostatic coupling between circuit elements and prevent cross-talk. Specially designed and fabricated semiconductor and printed circuit board materials are conventionally, however, more expensive than standard materials.

Isolation of regions or signal traces using grounding and capacitive planes have also been used to reduce electromagnetic coupling. One approach to reducing cross-talk, as illustrated in Figure 1, is to use a ground plane 2 on a substrate 4 to couple cross-talk 6 from a signal trace 8 to ground. Through the use of a ground plane 2, the signal traces 8 may be placed closer together than without the ground plane 2. A similar approach, shown in Figure 2, is to use a ground plane 2 and a relatively thinner substrate 10. By using a thinner substrate 10, the signal traces 8 are placed closer to the ground plane 2, and, as a result, may then be placed closer to each other. Thus, everything else being equal, placing the ground plane 2 closer to the signal traces 8 decreases coupling and impedance, and allows for closer spacing of signal traces 8, as shown in Figure 2.

U.S. Patent 5,451,917 to Yamamoto et al. (Sep. 19, 1995) discloses a high frequency circuit shielded from external interference through a series of grounding and capacitive layers surrounding dielectric circuit layers. U.S. Patent 5,371,653 to Kametani et al. (Dec. 6, 1994) discloses a multilayer circuit board comprising grounding layers

above and below each layer of signal traces, the ground layer being separated from the signal traces by insulative layers and further being thermally coupled to conductive grounding pins to release heat from the internal layers of the structure. U.S. Patent 4,626,889 to Yamamoto et al. (Dec. 2, 1986) discloses several configurations of signal trace conductors and conductor layers in a printed circuit board, the printed circuit board also having grounded layers above and below the configurations of signal trace conductors, separated from the signal trace conductors by insulative layers. U.S. Patent 5,945,886 to Millar (Aug. 31, 1999) also discloses a multilayer printed circuit board structure having a signal bus comprising straight signal traces of equal electrical length extending on a first layer of a printed circuit board and returning on a second layer of the printed circuit board. The first and second signal trace layers of the printed circuit board each have a distinct, adjacent ground plane. Coupled to each of the ground planes, Millar discloses additional straight signal traces parallel to, and of length equal to, the other signal traces. The additional signal traces are placed within a signal layer of the circuit board, in between the other parallel signal traces. The outer layers of the multi-layer structures disclosed by Millar include circuit traces. Similar to specially designed substrate layers, however, the more layers which are included on a substrate, the more expensive the substrate is to fabricate.

Therefore, it is desirable to have a substrate design which reduces or eliminates cross-talk in a variety of signal trace configurations, yet does not require expensive specialty substrate layers and designs, or extensive multiple layer systems used in the prior art.

SUMMARY OF THE INVENTION

The present invention provides a relatively inexpensive alternative to complex and specially fabricated substrates by placing voltage reference traces between each two signal traces to couple any electrostatic or electromagnetic "cross-talk" which would have occurred between the signal traces. By placing voltage reference traces between adjacent signal traces, cross-talk is effectively reduced without the expense and complexity of structures previously known in the art. According to a first aspect of the invention, each of a plurality of signal traces placed on a first surface of an electrically insulative

substrate are separated from the remaining signal traces by at least one voltage reference trace. This aspect of the invention may be further enhanced by placing a voltage reference plane on a second surface of the electrically insulative substrate, and optionally coupling each of the voltage reference traces to the voltage reference plane. The invention may also be applied to multiple layer circuit boards, optionally connecting portions of the various layers through vias. Signal trace vias may also be separated by voltage reference trace vias.

According to a second aspect of the invention, on an electrically conductive layer formed on an electrically insulative substrate, a portion of the electrically conductive material is removed to form conductive co-planar circuit traces separated from the remainder of the electrically conductive layer by a narrow trough or gap. The remainder of the substantially co-planar electrically conductive layer, excluding the circuit traces, may then be coupled to a reference voltage to couple electrostatic and electromagnetic fields from the circuit traces.

An electronic system is disclosed comprising a processor, a memory device, an input, an output and a storage device, at least one of which includes a printed circuit board or other substrate having two or more signal traces configured such that each two signal traces are separated by at least one voltage reference trace.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The nature of the present invention as well as other embodiments of the present invention may be more clearly understood by reference to the following detailed description of the invention, to the appended claims, and to several drawings herein, wherein:

Figure 1 is a diagram of a prior art substrate having signal traces spaced from a grounding layer by a thick insulating layer;

Figure 2 is a diagram of a prior art substrate having signal traces spaced from a grounding layer by a thin insulating layer;

Figure 3 is a diagram illustrating signal traces and voltage reference traces atop an insulating substrate according to an embodiment of the present invention;

Figure 4 is a diagram illustrating two adjacent circuit traces;

Figure 5 is a diagram illustrating signal traces and a voltage reference trace extending through a substrate via according to an embodiment of the present invention;

Figure 6 is a diagram of voltage reference traces placed between signal traces on the surface of a printed circuit board having a voltage reference plane according to an embodiment of the present invention;

Figure 7 is a diagram illustrating a multilayer substrate having signal traces and voltage reference traces atop an insulating substrate and voltage reference layer according to an embodiment of the present invention;

Figure 8 is a diagram of the surface of a printed circuit board having circuit traces on two surfaces of the circuit board according to an embodiment of the present invention;

Figure 9 is a diagram illustrating a multilayer substrate having multiple circuit traces configured according to an embodiment of the present invention;

Figure 10 is a diagram illustrating a multilayer substrate having multiple circuit traces configured according to another embodiment of the present invention;

Figure 11 is a diagram illustrating a flip-chip semiconductor die having circuit traces thereon configured according to an embodiment of the present invention;

Figure 12 is a top view of a substrate having circuit traces and a voltage reference bar thereon according to an embodiment of the present invention;

Figure 13 is a top view of a substrate having conductive regions around the circuit traces removed according to an embodiment of the present invention;

Figure 14 is a block diagram of an electronic system including a printed circuit board according to the present invention; and

Figure 15 is a diagram of a semiconductor wafer having circuit traces configured according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Figure 3 is a diagram illustrating a substrate 12, such as a printed circuit board ("PCB") or a semiconductor die, having circuit traces 14 thereon. The circuit traces 14 are formed using methods such as masking and etching, masking and deposition in mask

apertures, trace stamping, doping a substrate, or other methods well known in the art. As used herein, the term circuit "trace" refers not only to a surface conductive path which is conventionally formed upon the surface of a printed circuit board, but to any conductive path formed on, in or through a substrate such as a printed circuit board, thin film device or other semiconductor device. The circuit traces 14 of the present invention are primarily of two kinds, signal traces 16 and voltage reference traces 18. According to an embodiment of the invention shown in Figure 3, each signal trace 16 is separated from each adjacent signal trace 16 by at least one voltage reference trace 18. Thus, when signals are transmitted through any of the signal traces 16, cross-talk 20 which would have occurred between adjacent signal traces 16 is coupled by a voltage reference trace 18. By placing at least one voltage reference trace 18 between each two signal traces 16, cross-talk between signal traces 16 is effectively reduced without specially designed substrate materials or complex multiple layer substrates. Additionally, because conventional substrate fabrication methods already include a step, such as the aforementioned masking and etching, to form circuit traces 14, the present invention does not require any additional fabrication steps. Furthermore, for methods involving etching fluid, where a portion of a conductive layer is dissolved to form circuit traces, because more of the conductive layer is left on the substrate when forming the circuit traces of the present embodiment than is conventionally removed, less etching fluid is required, thereby reducing the cost of fabrication.

Electromagnetic coupling between circuit traces occurs primarily between adjacent circuit traces. In reference to Figure 4, the magnitude of the electromagnetic fields coupled, and the resulting current induced in an adjacent circuit trace 14, depends upon the space ("D") between the circuit traces 14, the material between the circuit traces 14, and the height ("H"), and therefore the laterally facing surface areas, of the circuit traces 14. By placing a voltage reference trace 18 (Figure 3) between each two signal traces 16, electromagnetic and electrostatic fields are coupled by the voltage reference trace 18 rather than a signal trace 16. Circuit trace forming fabrication technology presently allows for a minimum space of 40 μm between copper circuit traces having a height of 18 μm. The limitation on the spacing between circuit traces is related to the

isotropic etching process most preferably used to form the circuit traces. Because the traces are isotropically etched, the gap between the trace is at least two times the trace thickness. This ratio, however, will certainly improve as technology improves, and will be different for other technologies used.

The principles of the present invention are not limited to surface circuit traces. Cross-talk between conductive traces occurs any time a current-carrying conductive trace is placed near another conductive trace. Figure 5 shows a portion of a substrate 12, such as a printed circuit board, including two signal traces 16 separated by a voltage reference trace 18, wherein the three traces 16 and 18 extend through the substrate by vias 20. It is also contemplated that circuit traces may be extended to one or more of various layers of a substrate using vias configured according to the present invention rather than extending completely through the substrate 12 as shown in Figure 5.

A conductive trace may begin to exhibit properties similar to that of an antenna when extended for a distance without coupling to a reference voltage. Thus, it is preferable that the voltage reference traces placed between the signal traces are periodically coupled to a reference voltage. The voltage reference traces should at least be coupled to a reference voltage at the beginning and end of the trace. More preferably, however, the voltage reference traces are coupled to a reference voltage at predetermined intervals to maintain a substantially consistent reference voltage throughout the extent of the trace. Figure 6 illustrates a substrate 12 having voltage reference traces and signal traces 16 and 18 on the surface thereof, each of the voltage reference traces 18 being coupled to a ground plane 22 on another surface of the substrate 12 through vias 20. By periodically coupling voltage reference traces 18 to a reference voltage plane 22 along the extents of the voltage reference traces 18, a more consistent reference voltage is maintained to more effectively reduce cross-talk between the signal traces 16. As shown in Figure 7, the principles of this invention also work with multilayer substrates 12 having a reference voltage plane 22 placed between two electrically insulative substrate layers 12. The voltage reference traces 18 from each outer surface 21 of the overall substrate may be coupled to the voltage reference plane 22 through vias 20.

As shown in Figure 8, for substrates 12 having traces 16 and 18 on more than one surface of the substrate, a voltage reference trace 18 may be placed between each two signal traces 16 for signal traces 16 on both surfaces of the substrate 12. For the embodiment shown in Figure 8, the signal traces 16 on a first surface 21 of the substrate 18, in addition to being adjacent to a voltage reference trace 18 on the first surface 21 of the substrate 12, are adjacent a voltage reference trace 18 on the second surface of the substrate 12. By configuring the traces 16 and 18 so that no signal trace 16 is directly adjacent any other signal trace 16, cross-talk is most substantially reduced. The embodiment of Figure 8, wherein multiple layers of signal traces 16 are placed such that they are not adjacent to any other signal traces 16, may also be implemented in substrates having one or more signal traces on a layer within the substrate 12. Figure 9 illustrates an embodiment of the present invention wherein voltage reference traces 18 are placed between each two signal traces 16 such that no signal trace 16, whether on a common, or different substrate layer 12 of the overall substrate, are placed immediately adjacent another signal trace 16. Figure 10 illustrates an embodiment of the present invention wherein voltage reference traces 18 placed on or between different substrate layers 12 may be connected through vias 20. Signal traces 16 may also be coupled by vias 20 through a substrate layer 12.

Figure 11 illustrates an embodiment of the present invention wherein circuit traces 24 are placed on the surface of a semiconductor substrate 24, more particularly in a flip-chip ball grid array ("BGA") application. Like previous embodiments, the circuit traces 24 are configured such that a voltage reference trace is placed between each two signal traces so that no signal trace is placed immediately adjacent another signal trace.

As illustrated by Figure 12, for embodiments of the invention where no voltage reference plane is used, or in addition to a voltage reference plane, one or more voltage reference terminals, bars or buses 30 may be placed upon the substrate 32 at a point or points from or to which the voltage reference traces 34 may extend. As with previous embodiments, the voltage reference traces 34 of the present embodiment are placed between each two adjacent signal traces 36 such that no two signal traces 36 are immediately adjacent. Additionally, the voltage reference traces 34 may be coupled to

additional voltage reference terminals, bars or buses 30 at various points along their extents to reduce the extent to which the voltage reference traces 34 act as antennas. This configuration of circuit traces may also be placed between substrate layers as may be required for a particular application.

Rather than forming distinct voltage reference traces on a substrate, conductive material from a conductive layer of the substrate may be removed only from portions immediately surrounding a desired signal trace location to create an electrically isolating trough or gap 40 between the signal trace 38 and the remainder 42 of the conductive material on the substrate 32. As shown in Figure 13, a layer of conductive material on a substrate 32 has been removed only around the co-planar signal traces 38. Methods of removing selected portions of conductive material from a substrate, such as by masking and etching, are well known in the art. By leaving a majority of the conductive material on the substrate 32, etching solution is preserved. Furthermore, by connecting the remaining conductive material 42, other than the co-planar signal traces 38, to a reference voltage, the electromagnetic or electrostatic field emanating from a signal trace 38 will not be coupled by an adjacent signal trace 38, but will be coupled by the conductive material remaining 42 and between each of the signal traces 38. This aspect of the invention may also be applied to substrates having multiple conductive layers such as those described with regard to Figures 6-10. As will be clear to one of ordinary skill in the art, a region around the solder pads of a printed circuit board, or any other point where the signal traces connect with an external component, should be clear of conductive material for a region sufficient to avoid solder flow shorting the signal trace to the conductive material. The size of the cleared region required will depend upon the particular signal trace layout, bond pad size and soldering techniques used, but may be readily determined by one of ordinary skill in the art. As will also be clear to one of skill in the art, a passivation layer may be placed over a conductive layer to reduce the likelihood of shorts between the conductive traces due to dust or other debris. Passivation layers and methods of applying them are well known in the art.

Figure 14 is a block diagram of an electronic system 100 which includes components having one or more printed circuit boards 106 or other substrates comprising

circuit traces configured according to one or more embodiments of the present invention. The electronic system 100 includes a processor 104 for performing various computing functions, such as executing specific software to perform specific calculations or tasks. Additionally, the electronic system 100 includes one or more input devices 108, such as a keyboard or a mouse, coupled to the processor 104 to allow an operator to interface with the electronic system 100. The electronic system 100 also includes one or more output devices 110 coupled to the processor 104, such output devices including such outputs as a printer, a video terminal or a network connection. One or more data storage devices 112 are also conventionally coupled to the processor 104 to store or retrieve data from external storage media (not shown). Examples of conventional storage devices 112 include hard and floppy disks, tape cassettes, and compact disks. The processor 104 is also conventionally coupled to a cache memory 114, which is usually static random access memory ("SRAM"), and to DRAM 102. It will be understood, however, that the printed circuit board 106 or other substrate configured according to one or more of the embodiments of the present invention may be incorporated into any one of the cache, DRAM, input, output, storage and processor devices 114, 102, 108, 110, 112, and 104.

As shown in Figure 15, circuit traces 118 may be fabricated on the surface of a semiconductor wafer 116 of silicon, gallium arsenide, or indium phosphide in accordance with one or more embodiments of the present invention. One of ordinary skill in the art will understand how to adapt such designs for a specific chip architecture or semiconductor fabrication process. Of course, it should be understood that the circuit traces 118 may be fabricated on semiconductor substrates other than a wafer, such as a Silicon-on-Insulator (SOI) substrate, a Silicon-on-Glass (SOG) substrate, a Silicon-on-Sapphire (SOS) substrate, or other semiconductor material layers on supporting substrates.

Although the present invention has been shown and described with reference to particular preferred embodiments, various additions, deletions and modifications that are obvious to a person skilled in the art to which the invention pertains, even if not shown or specifically described herein, are deemed to lie within the scope of the invention as encompassed by the following claims.

CLAIMS

What is claimed is:

1. A printed circuit board comprising:

a substrate having at least one electrically insulative layer; and

at least two conductive trace layers formed on opposing sides of the at least one electrically insulative layer, wherein at least one of the at least two conductive layers includes at least two signal traces and at least one voltage reference trace, the conductive traces being configured such that at least one voltage reference trace is between each two signal traces.

2. The printed circuit board of claim 1, wherein at least one conductive trace includes at least one direction change in its length over the at least one electrically insulative layer.

3. The printed circuit board of claim 1, wherein the at least one electrically insulative layer comprises a plurality of insulative layers, each separated by at least one conductive trace layer.

4. The printed circuit board of claim 1, wherein at least one of the conductive trace layers is a voltage reference plane.

5. The printed circuit board of claim 4, wherein the at least one voltage reference trace is coupled to the voltage reference plane.

6. The printed circuit board of claim 1, further comprising a passivation layer deposited on at least one of the conductive trace layers.

7. The printed circuit board of claim 1, wherein the at least one electrically insulative layer is two electrically insulative layers separated by a conductive layer, and wherein the at least one voltage reference trace is electrically coupled to the conductive layer.

8. The printed circuit board of claim 1, wherein at least one of the at least two conductive trace layers further comprises at least one voltage reference bus, wherein the at least one voltage reference trace is electrically coupled to the at least one voltage reference bus.

9. The printed circuit board of claim 1, wherein at least a portion of the conductive traces are embodied as vias.

10. A printed circuit board comprising at least one electrically insulative layer and at least one electrically conductive layer, the electrically conductive layer comprising at least one signal trace electrically isolated from a voltage reference portion, wherein the voltage reference portion has a greater surface area than the at least one signal trace.

11. The printed circuit board of claim 10, wherein a majority of the electrically conductive layer is comprised in the voltage reference portion.

12. The printed circuit board of claim 10, wherein the voltage reference portion comprises a voltage reference bus having voltage reference traces extending therefrom.

13. An electronic device comprising:

at least one electrically insulative layer; and

at least one conductive layer, the conductive layer comprising a voltage reference bus having at least one voltage reference trace extending therefrom and at least two signal traces electrically isolated from the at least one voltage reference trace, wherein the at least one voltage reference trace and at least two signal traces are configured such that each signal trace is separated from each other signal trace by at least one voltage reference trace.

14. The electronic device of claim 13, further comprising a passivation layer deposited on at least one of the at least one conductive layer.

15. A printed circuit board comprising:

at least one voltage reference plane substantially coextensive with a portion of a substrate; and

at least one signal trace substantially co-planar with the voltage reference plane and electrically isolated therefrom, the voltage reference plane having a substantially greater surface area than any one signal trace.

16. The printed circuit board of claim 15, wherein the at least one signal trace is electrically isolated from the at least one voltage reference plane by at least one trough.

17. The printed circuit board of claim 15, further comprising a passivation layer deposited on the at least one signal trace and the at least one electrically insulative layer.

18. The printed circuit board of claim 15, wherein the at least one voltage reference plane is a substantially continuous voltage reference plane.

19. A printed circuit board comprising at least one voltage reference plane having at least one co-planar signal trace isolated therefrom, wherein the at least one voltage reference plane includes a surface area greater than any one signal trace.

20. An electronic system comprising:

a processor;

a memory device associated with the processor; and

at least one of an input device, an output device and a data storage device associated with the processor;

wherein at least one component of the electronic system comprises at least two conductive trace layers formed on opposing sides of at least one electrically insulative layer, wherein each of the at least two conductive trace layers includes at least two signal traces and at least one voltage reference trace, the conductive traces being configured such that at least one voltage reference trace is between each two signal traces.

21. The electronic system of claim 20, wherein at least one of the at least two signal traces includes at least one non-linear path in its extent over the at least one electrically insulative layer.

22. An electronic system comprising:

a processor;

a memory device associated with the processor; and

at least one of an input device, an output device and a data storage device associated with the processor;

wherein at least one component of the electronic system comprises a voltage reference plane substantially coextensive with a portion of a substrate and at least one signal trace substantially co-planar with and electrically isolated from the voltage reference plane, the voltage reference plane having a surface area greater than the at least one signal trace.

ABSTRACT OF THE DISCLOSURE

A method and apparatus for substantially reducing or eliminating electromagnetic and electrostatic coupling between signal traces on a substrate is disclosed. A substrate, such as a printed circuit board, is formed with an electrically insulative layer and a conductive layer. A portion of the conductive layer is removed to form circuit traces including signal traces and voltage reference traces configured such that each signal trace is separated from each other signal trace by at least one voltage reference trace. The invention is also applied to multiple layer printed circuit boards including a single voltage reference plane, an electronic system, and a semiconductor substrate. According to another aspect of the invention, a majority of a conductive layer is left on an insulative layer of a substrate by removing only those portions of the conductive layer immediately adjacent signal traces such that the remaining conductive material, which is ordinarily removed, acts to couple electromagnetic and electrostatic fields from the signal traces.

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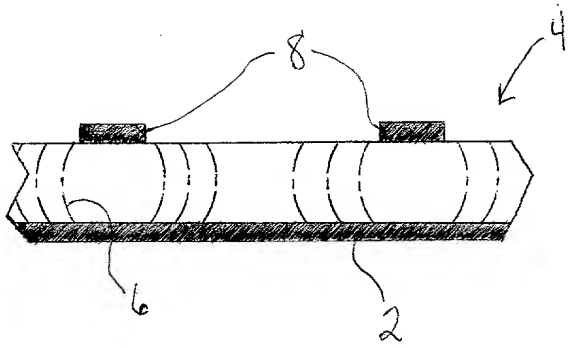


Figure 1 (Prior Art)

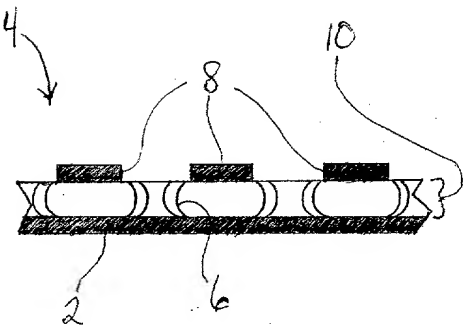


Figure 2 (Prior Art)

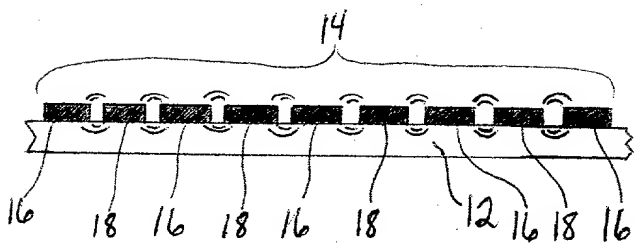


Figure 3

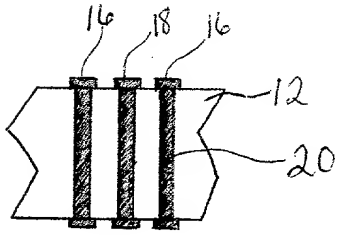


Figure 5

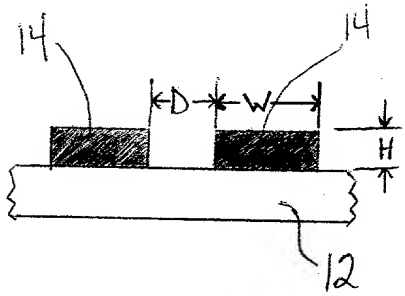
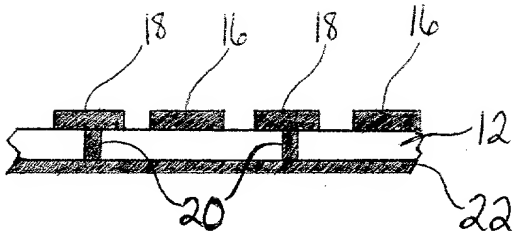


Figure 4



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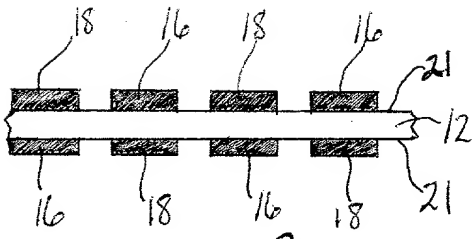

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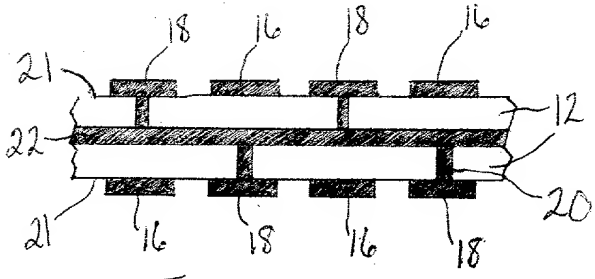

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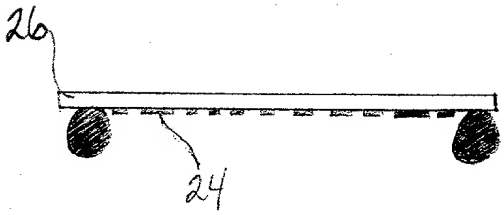


Figure 11

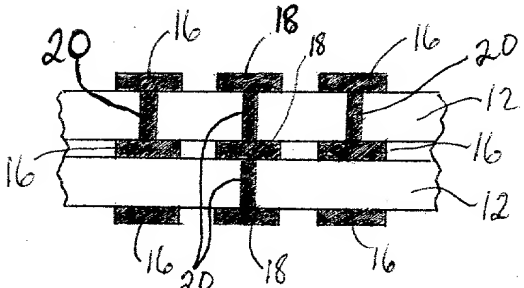


Figure 10

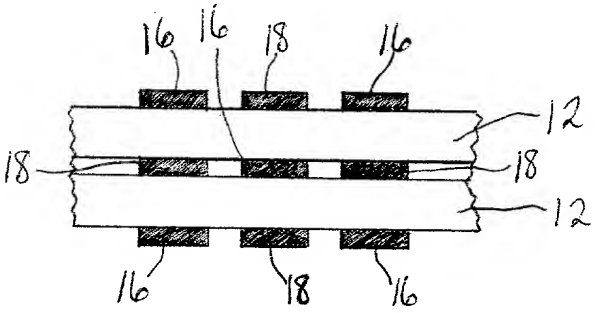
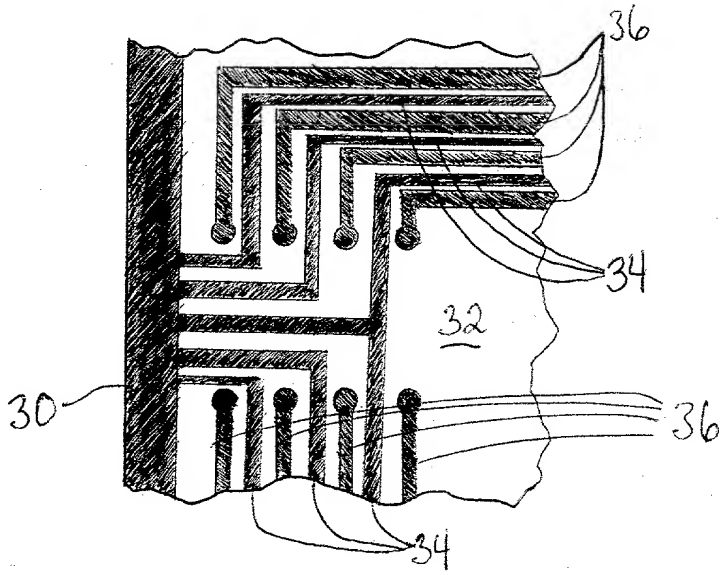


Figure 9



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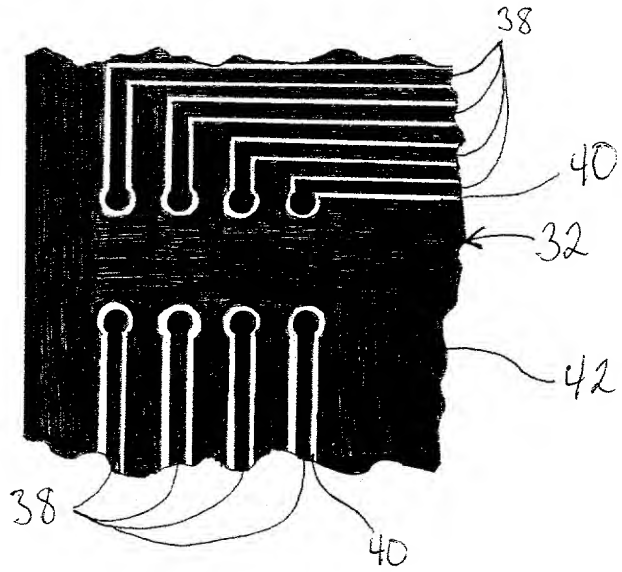

Figure 13

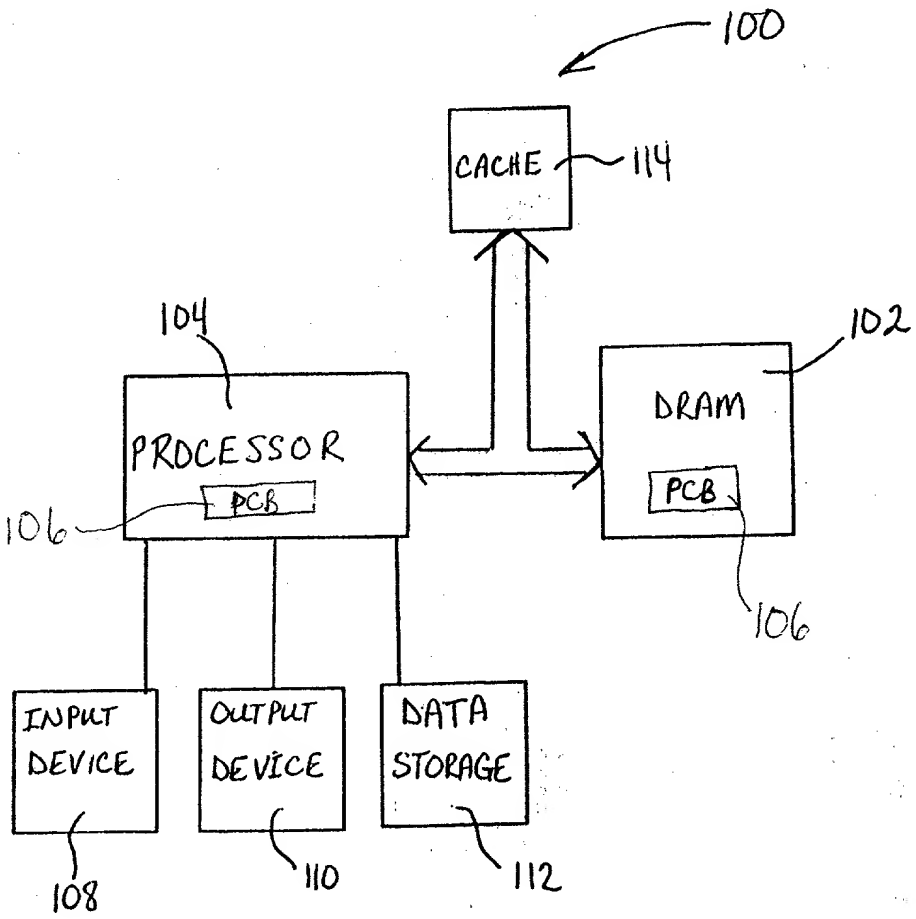

Figure 14

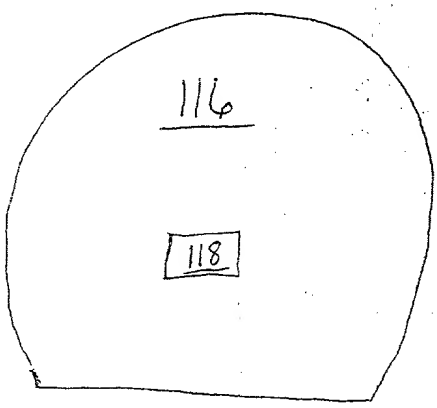

Figure 15

DECLARATION FOR PATENT APPLICATION (WITH POWER OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled METHOD AND APPARATUS OF INTERPOSING VOLTAGE REFERENCE TRACES BETWEEN SIGNAL TRACES IN SEMICONDUCTOR DEVICES, the specification of which (check one):

- ☒ is attached hereto.
- ☐ was filed on _____ as United States application serial no. _____ and was amended on _____.
- ☐ was filed on _____ as PCT international application no. _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

(number)	(country)	(day/month/year filed)	Priority Claimed Yes	No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application:

(application serial no.)	(filing date)	(status - pending, patented or abandoned)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

(provisional application no.)	(filing date)

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

David V. Trask, Reg. No. 22,012
Laurence B. Bond, Reg. No. 30,549
Allen C. Turner, Reg. No. 33,041
Stephen R. Christian, Reg. No. 32,687
Paul C. Oestreich, Reg. No. 44,983
Kenneth C. Booth, Reg. No. 42,342
Kerry D. Tweet, Reg. No. 45,959
William S. Britt, Reg. No. 20,969
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Samuel E. Webb, Reg. No. 44,394
Michael L. Lynch, Reg. No. 30,871
Thomas J. Rossa, Reg. No. 26,799
James R. Duzan, Reg. No. 28,393
Edgar R. Cataxinos, Reg. No. 39,931
Kenneth B. Ludwig, Reg. No. 42,814
Eleanor V. Goodall, Reg. No. 35,162
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Lia M. Pappas, Reg. No. 34,095

Address all correspondence to:

Joseph A. Walkowski, telephone no. (801) 532-1922.
TRASK, BRITT & ROSSA
P.O. BOX 2550
Salt Lake City, Utah 84110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole inventor: Warren M. Farnworth
Inventor's signature _____ Date 4-10-00
Residence: Nampa, Idaho
Citizenship: U.S.A.
Post Office Address: 2004 S. Banner, Nampa, ID 83686-7271

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Warren M. Farnworth	**Examiner:**	Unknown
Serial No.:	Not Yet Assigned	**Group Art Unit:**	Unknown
Filed:		**Attorney Docket No.:**	4161US (98-1265)
Title:	METHOD AND APPARATUS OF INTERPOSING VOLTAGE REFERENCE TRACES BETWEEN SIGNAL TRACES IN SEMICONDUCTOR DEVICES		

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

MICRON TECHNOLOGY, INC., assignee of the entire right, title and interest by assignment from the inventor(s) in the above-identified application, hereby appoints the following attorneys and agents:

David V. Trask, Reg. No. 22,012	William S. Britt, Reg. No. 20,969	Thomas J. Rossa, Reg. No. 26,799
Laurence B. Bond, Reg. No. 30,549	Joseph A. Walkowski, Reg. No. 28,765	James R. Duzan, Reg. No. 28,393
Allen C. Turner, Reg. No. 33,041	Kent S. Burningham, Reg. No. 30,453	Edgar R. Cataxinos, Reg. No. 39,931
Stephen R. Christian, Reg. No. 32,687	Brick G. Power, Reg. No. 38,581	Kenneth B. Ludwig, Reg. No. 42,814
Paul C. Oestreich, Reg. No. 44,983	Devin R. Jensen, Reg. No. 44,805	David L. Stott, Reg. No. 43,937
Kenneth C. Booth, Reg. No. 42,342	Samuel E. Webb, Reg. No. 44,394	Kerry D. Tweet, Reg. No. 45,959
Eleanor V. Goodall, Reg. No. 35,162	Michael L. Lynch, Reg. No. 30,871	Lia M. Pappas, Reg. No. 34,095

as its attorneys with full power of substitution to prosecute this application and all applications claiming filing date priority therefrom and to transact all business in the U.S. Patent and Trademark Office in connection therewith.

The above-identified assignee hereby elects, pursuant to 37 C.F.R. § 3.71, to conduct the prosecution of the above-identified patent application to the exclusion of the inventor(s).

A chain of title from the inventor(s) of the above-identified patent application to the above-identified assignee is shown:

[] In an assignment recorded in the U.S. Patent and Trademark Office at Reel , Frame .

[X] In an assignment filed herewith for recordation, a true copy of which is attached hereto.

The undersigned has reviewed the above-identified assignment and, to the best of his knowledge and belief, title is in the above-identified assignee.

The undersigned further avers that he is empowered to make and sign the foregoing certification on behalf of the above-identified assignee, and to take the action set forth herein on its behalf.

Please direct all communications regarding the above-identified application to:

Joseph A. Walkowski,
TRASK, BRITT & ROSSA
P.O. Box 2550
Salt Lake City, UT 84110
Tele: (801) 532-1922
Fax: (801) 531-9168

Respectfully Submitted,

MICRON TECHNOLOGY, INC.

Date: April 11, 2000

By: [signature]
Michael L. Lynch, Esq.
Reg. No. 30,871
Chief Patent Counsel,
MICRON TECHNOLOGY, INC.

N:\2269\4161\POA by Assignee.wpd

United States Patent & Trademark Office

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